

TB/05/00338



INVESTOR IN PEOPLE

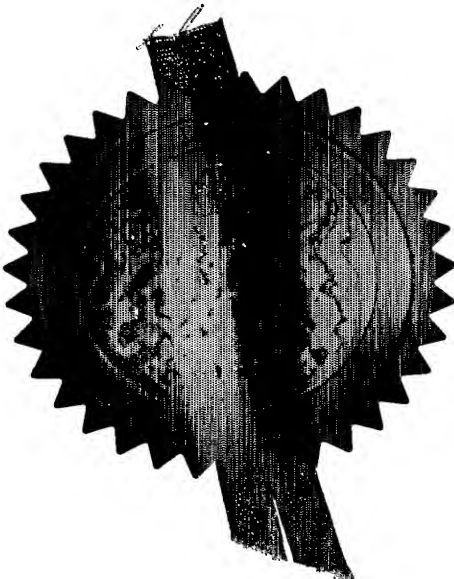
The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.



Signed

Dated 10 February 2005

**PRIORITY
DOCUMENT**

SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH RULE 17.1(a) OR (b)

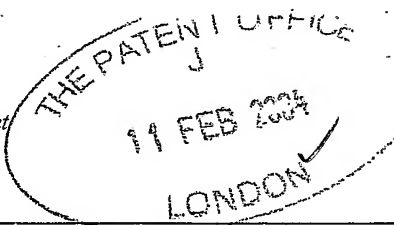


The
Patent
Office

The Patent Office
Cardiff Road
Newport
Gwent NP9 1RH

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)



1. Your reference
305010GB/DJW/ac

2. Patent application number
(The Patent Office will fill in this part)
11 FEB 2004 0403021.9 ✓

3. Full name, address and postcode of the or of each applicant (underline all surnames)
Nujira Ltd
Unit 6 and 7
Grange Park
Broadway, Bourn
Cambridge
CB3 7TA
12FEB04 E872537-11 002525
F01/7700 0.00-0403021.9 CHEQUE

Patents ADP number (if you know it) 08570715002

If the applicant is a corporate body, give the country/state of its incorporation
United Kingdom

4. Title of the invention
RESONANCE SUPPRESSION FOR POWER AMPLIFIER OUTPUT NETWORK

5. Name of your agent (if you have one)
"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)
PAGE WHITE & FARRER
54 DOUGHTY STREET
LONDON
WC1N 2LS
UNITED KINGDOM

Patents ADP number (if you know it) 1255003 ✓

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number

Country	Priority application number (if you know it)	Date of filing (day / month / year)

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing (day / month / year)

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (Answer 'Yes' if:
a) any applicant named in part 3 is not an inventor; or
b) there is an inventor who is not named as an applicant; or
c) any named applicant is a corporate body
See note (d))
YES



Patents Form 1/77

Enter the number of sheets for any of the following items you are filing with this form.
Do not count copies of the same document

Continuation sheets of this form 0

Description 11

Claim(s) 2

Abstract 1

Drawing(s) 5 ¹⁵

10. If you are also filing any of the following, state how many against each item.

Priority documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (Patents Form 7/77)

Request for preliminary examination and search (Patents Form 9/77)

Request for substantive examination (Patents Form 10/77)

Any other documents
(please specify)

11. I/We request the grant of a patent on the basis of this application.

Signature

Date

PAGE WHITE & FARRER 11 February 2004

12. Name and daytime telephone number of person to contact in the United Kingdom

David J Williams 020 7831 7929

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

- a) If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.
- b) Write your answers in capital letters using black ink or you may type them.
- c) If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.
- d) If you have answered 'Yes' Patents Form 7/77 will need to be filed.
- e) Once you have filled in the form you must remember to sign and date it.
- f) For details of the fee and ways to pay please contact the Patent Office.



RESONANCE SUPPRESSION FOR POWER AMPLIFIER OUTPUT NETWORK

Field of the Invention

The present invention relates to power amplifiers, and in particular a power amplifier provided with a modulatable power supply.

Background to the Invention

A known technique for providing an efficient means of power amplifying a non-constant envelope signal is to use envelope modulation. Envelope modulation is typically provided by means of a highly efficient modulatable power supply.

However, in such an arrangement the power amplifier presents an impedance to the modulatable supply. In particular, this impedance can change rapidly with frequency due to a presence of a high Q series resonance, making accurate high bandwidth modulation very difficult. In a typical transistor output stage, the transistor device capacitance resonates with the inductance of the supply feed to form such a series resonance. This series resonance presents problems if the supply modulation is to be applied at high bandwidths.

One solution is to redesign the power output stage to move the resonance to a higher frequency. However it is difficult to achieve this without compromising the output stage with respect to some other parameter. For example reducing the capacitance can only be achieved by changing the output device technology from, for example, LDMOS to GaAs mesfet or Phemt. This could potentially have a major implication on the cost of such units, as well as the ability to manufacture such units. Reducing the inductance of the supply feed, as an alternative, would affect the load presented to the transistor at RF and its harmonics. This could compromise the RF stage efficiency, gain or bandwidth.

Thus a problem exists with current power amplifier output stages in that at high frequencies a series resonance is presented at the power supply terminal of the

amplifier as a consequence of the output capacitance of the transistor forming a high Q resonant network with the supply feed inductance. This network creates a source of potential instability, and creates a long time constant energy storage means that contributes to memory effect, and renders any form of wideband envelope modulation difficult to apply.

It is an aim of the present invention to provide an improved technique which addresses one or more of the above stated problems.

Summary of the Invention

In accordance with the invention there is provided a power amplifier including a resistive element connected at an output thereof to maintain a low impedance at the output across a range of operational frequencies.

The power amplifier may further include a transistor for receiving a signal to be amplified at an input and for providing an amplified signal at the output.

The output may be adapted for connection to a modulated power supply. The output may be adapted for connection to a modulated power supply via a supply feed inductance.

Said resistive element may comprise a resistor.

A reactive element may be connected in series with said resistive element. The resonant element may comprise a capacitive element or an inductive element in series with a capacitive element. Said inductive element may comprise a conductive element of said circuit. The conductive element may comprise a part of a conductive track or a bond wire. Said inductive element may comprise an inductor. Said capacitive element may comprise a capacitor.

The signal to be amplified may be a radio frequency signal.

In a further aspect the invention provides a power amplifier circuit comprising a transistor for receiving a signal to be amplified at an input and for outputting an amplified signal at an output; a modulated power supply connected to the transistor output; and a resistive element connected at the transistor output such that a low

impedance is maintained at the transistor output across a range of operational frequencies.

The invention still further provides a method of maintaining a low impedance across a range of operational frequencies in a power amplifier, the method including providing a resistive element at an output of the power amplifier.

The method may further comprise step of providing a reactive element connected in series with said resistive element.

A series resonance at the power supply is equivalent to a parallel resistance at the junction between the inductance and the capacitance. This junction is the drain of the transistor. The low impedance at the power supply terminal is equivalent to a high impedance at the transistor terminal. This provides a solution of presenting a low impedance to the transistor terminal to thereby damp out the series resonance appearing at the power supply terminal.

Brief Description of the Figures

The invention is now described with reference to particular embodiments as illustrated by the accompanying figures, in which:

Fig. 1 illustrates a physical representation of a RF power stage, including example locations of a control circuit implemented in accordance with embodiments of the invention;

Fig. 2 illustrates the equivalent circuit of a packaged power transistor such as shown in Fig. 1;

Figs. 3(a) to 3(c) illustrate curves of impedance, phase, and amplitude respectively for various frequencies, exhibited by the resonance at the transistor terminal with and without a control circuit in accordance with embodiments of the invention;

Figs. 4(a) and 4(b) illustrate the electrical equivalent circuit of a power amplifier such as shown in Fig. 1, including the implementation of a control circuit in accordance with embodiments of the invention; and

Fig. 5 illustrates the implementation of a particular embodiment of a control network in accordance with the invention in a power amplifier output network.

Description of the Preferred Embodiments

5 With reference to Fig. 1, an example physical representation of a RF power stage with which embodiments of the invention is implemented is illustrated.

With reference to Fig. 1, reference numeral 140 generally represents a transistor package. Reference numeral 102 generally represents the top surface of the transistor package. The jagged line 142 represents the opening of the top
10 surface of the transistor package to show at least part of the internal structure thereof. The internal structure of the transistor package includes an array of transistor power amplifiers 114 and a corresponding array or bank of matching capacitors 108. The plurality of transistor power amplifiers 114 are connected to the corresponding plurality of capacitors 108 via a plurality of bond wires 110. The
15 plurality of capacitors 108 are connected, via a further plurality of bond wires 112, to a metallisation 116 which represents the connection of the bond wires 112 external to the transistor package 140. The transistor package additionally is provided with a metallisation 106 which is connected to ground, as represented by reference numeral 104. A plurality of inputs are provided to the transistor package, forming the inputs
20 for the plurality of transistor power amplifiers 114. The plurality of inputs are generally represented by reference numerals 138.

As the invention is concerned with the output of the transistor amplifiers, as further described hereinbelow, the input stages of the transistor package 140 are not shown in any detail in Fig. 1.

25 As further illustrated in Fig. 1, there is provided a metallisation pattern 132 on a printed wiring board or printed circuit board on which the transistor package 140 is mounted. The metallisation 116 connected to the bond wires 112 connect to the metallisation layer 132 on the printed wiring or circuit board.

The metallisation 132 is configured to have a bias feed strip 138 to which a DC
30 supply voltage is supplied, a transistor drain strip 134, and an output strip 136 at which the radio frequency output signal RF_{OUT} is provided.

The DC feed 138 provides a defined load for the RF transistor and the RF frequency and harmonics thereof. Ideally, this load would be a short at baseband frequencies. However in order to provide a satisfactory load at the radio frequency and harmonics thereof, the baseband impedance is required to be significant.

5 In order to provide an acceptable match to the low internal load impedance of the output of the transistor, an internal match network is typically provided internal to the transistor. This is best illustrated by an equivalent circuit of the power amplifier circuit, as represented in Fig. 2.

Fig. 2 shows a typical equivalent circuit of the output of a power amplifier circuit including the elements internal to the transistor package 102.

As represented in Fig. 2, the equivalent circuit includes a transistor 210. A capacitor 206 is connected in parallel across the source and drain of the transistor. The capacitor 206 represents the internal parasitic capacitance to the bulk of the transistor 210. The output of the transistor 210, namely the transistor drain, is taken on line 212 and connected to the DC power supply. It should be noted that the DC supply is connected to the output of the transistor via a supply feed inductance (not shown in Figures 1 and 2). A series inductance, represented by inductor 202, is connected to the drain of the transistor 210. This inductor 202 is representative of the inductance of the bond wire 110 connecting the output of the transistor power amplifier to a capacitor of the capacitor bank 108. A capacitor 208 is connected in parallel across the inductor 202 and the source of the transistor 210. The capacitor 208 represents one of the capacitors of the capacitor bank 108. A further inductor 204 is connected in series with the inductor 202. The inductor 204 represents the inductance of the bond wire 112 connecting the capacitor 208 to the metallisation 116. The source of the transistor 210 is connected to ground, represented by reference numeral 214. In Fig. 2, the terminal 216 represents the connection to the metallisation 116, and the terminal 218 represents a ground connection.

In transistor power amplifier implementations, the capacitor bank 108 may not always be provided. The capacitor bank 108 provides an impedance transformation capacitor for each transistor power amplifier. Where the capacitor bank 108 is not provided, use of the invention, as further described hereinbelow, is still

advantageous, because there is still substantial capacitance associated with the transistor structure, as represented by capacitor 206 in Fig. 2.

As can be seen from Fig. 2, the equivalent circuit of the transistor package provides a resonant circuit. The resonant circuit has contributions to capacitance from the bulk capacitance 206 and the matching capacitor 208 from the capacitor bank 108. The inductance includes inductors 202 and 204 representing the inductance of the bond wires 110 and 112, as well as the supply feed inductance. In addition, the inductance is further contributed to by the transistor drain strip 132 and the bias feed 138. This inductance all appears across the supply in series with the capacitors 206 and 208. This parasitic resonant circuit results in parasitic resonance at high impedance, when a high impedance is presented at the transistor output.

The structure of the power amplifier circuitry provides a series resonant network at the power supply terminal, leading to the presentation of a very low impedance load to the power supply at high frequencies. This low impedance presented to the power supply transforms into a high impedance presented to the transistor drain. The resonance is undesired. In order to provide damping to this undesired resonance, a low resistance can be provided to the drain of the transistor for the same range of frequencies that the bias network presents a high impedance. However, this must be achieved without loading the output of the transistor at radio frequencies. If envelope modulation is to be applied, the network must also not provide significant loading at the modulation frequency.

The inventive solution is to provide a resistor in series with the DC feed to reduce the Q of the resonance. This is an effective solution, but a resistor set at a value that significantly reduces the resonance may consume an unexpectedly large portion of the power fed to the amplifier.

The invention thus provides a solution by providing a second resonant network, which may be considered to be a resonance compensation network or circuit or a control network or circuit, that connects to the output of the transistor. As the impedance of the transistor output terminal rises due to the bias resonance, the control resonant network impedance lowers.

The problem to which the invention is addressed, and the solution provided by the invention, is further discussed with reference to Figs. 3(a) to 3(c), before further describing the implementation of the solution with regards to Figs. 4(a) and 4(b) and Fig. 5.

Fig. 3(a) illustrates a plot of impedance against frequency for a transistor power amplifier with a modulatable supply. Reference numeral 302 designates the plot of impedance against frequency of such an amplifier output stage without any compensation in accordance with the invention. As can be seen, a spike 312 occurs at a particular range of frequencies, causing a significantly increased impedance at such frequencies. The impedance characteristics provided by the compensation circuit, the structure of which is further described hereinbelow, is represented by the curve 304. As can be seen, the curve 304 represents a significantly lower impedance at the range of frequencies at which an impedance problem occurs. As a result, the overall effect of the control circuit is such that at the range of frequencies where the impedance ordinarily is significantly increased, the impedance is reduced. As illustrated in Fig. 3(a), the effect of the control circuit between points 306 and 308 on the curve 302 is denoted by the dash line 310, and it can be seen that the impedance is substantially reduced.

With reference to Fig. 3(b), there is illustrated a plot of phase against frequency for the transistor output amplifier. As can be seen, the plot 317 has a significant negative peak denoted by reference numeral 316. By provision of the control circuit of the present invention, this peak is removed and the curve has a much reduced distortion between points 318 and 320 as represented by dash line 322. Similarly in Fig. 3(c) there is illustrated a plot of amplitude against frequency. As can be seen the output amplitude dips significantly to a negative peak at point 314. The curve of amplitude against frequency 319 is controlled by the control circuit of the invention between points 324 and 326 such that the negative peak is significantly reduced, as represented by the dash line 328.

The invention, and the example implementation thereof, is now further illustrated with reference to Figs. 4(a) and 4(b). In Fig. 4(a), a transistor power amplifier is represented by reference numeral 402. A capacitor 406, representing a

matching capacitance, is connected in parallel across the source and drain of the transistor 402. Resistor 404 represents a load which the power amplifier is driving. Further represented in Fig. 4(a) are four inductors, denoted 412, 410, 408, and 407. The inductor 407 represents the inductance associated with the supply strip 138, the inductor 408 represents the inductance associated with the metallisation 132 between the connection point to the metallisation and the supply strip, the inductor 410 represents the inductance of the metallisation between the connection point to the metallisation and the drain strip 134, and the inductor 412 represents the inductance of the drain strip 134. The points A, B, C, D are marked in Fig. 4(a) and in Fig. 1, and the inductors 412, 410, 408, 407 represent the inductances between such points, which are provided by metallisation.

The invention, in embodiments, is to provide a resonant circuit at the output of the transistor power amplifier. Such a resonant circuit is illustrated in Fig. 4(b). The resonant circuit 426 comprises, in series, an inductor 420, a capacitor 422, and a resistor 424. The resonant circuit 426 is connected between terminals 428 and 430, and terminal 430 is connected to ground as represented by reference numeral 432. The provision of the resistor 424 allows the power problem as described hereinabove to be avoided. The resonant circuit provided by the inductor 420 and the capacitor 422 are not required in order to overcome the power problem, but are preferably provided so as to ensure that the resistor 424 does not consume power.

In various embodiments, the control circuit of the invention, as represented by the resonant circuit 426 of Fig. 4(b), may be connected at any one of the points A, B, C, D shown in Figs. 1 and 4(a). Specifically, the terminal 428 may be connected to any one of the points A, B, C, D. These points represent the possible locations of the control circuit, or being locations of the output of the transistor power amplifier.

There are different advantages associated with the provision of the control circuit at ones of the various points. As can be seen from Figs. 1 and 4(a), the closer the control circuit 426 is connected to the DC supply, the higher the value of the inductor 420 is required. A particularly advantageous location of the control circuit 426 is to connect the terminal 428 at point D, denoted by reference numeral 130 in Fig. 4(a). In such location, the series inductance provided by the inductors 407, 408,

410, 412 is such that the inductor 420 can be eliminated, and the control circuit 426 may comprise simply a capacitor 422 and a resistor 424. In such location of the control circuit, the inductors 407, 408, 410, 412 provide the inductance of the resonant circuit. Thus, it will be understood that whether the resonant circuit is
 5 required to specifically have an inductor component is dependent upon the size of the inherent inductance provided in the circuit implementation. The inductance of the control circuit may simply be provided by the inherent inductance within the circuit, and such inherent inductance becomes part of the circuit.

It should be noted that in Fig. 1 the points A, B, C, D are provided by way of
 10 example. As discussed hereinabove, point D has significant advantages insofar as that the inductance provided by the metallisation between the DC supply and point D is such that no specific inductor 420 may be required in a control circuit 426. It will also be understood that the points A, B, C, D are not the only points at which the control circuit may be applied. The control circuit may be applied at any point at the
 15 output stage. The points A, B, C, D are represented by reference numerals 126, 124, 128, 130 in Fig. 4(a). It will be understood that if any of these points move along the metallisation, either away from or toward the DC supply, then the inductance values of the inductors 407, 408, 410, 412 will vary. It should be noted that point B, denoted by reference numeral 124, represents the point at which the bond wire 112 connects
 20 with the metallisation layer 132 on the printed wiring or circuit board.

A further embodiment of the invention is illustrated in Fig. 5, which more fully illustrates an implementation of the output stage of a transistor power amplifier. In Fig. 5, the transistor power amplifier is denoted by reference numeral 502.

Reference numeral 504 denotes a matching network connected to the output of the
 25 transistor through which the radio frequency output of the power amplifier is generated on line 512. The matching network comprises a series pair of inductors 508 and 506, and a parallel capacitor 510 connected to ground. The modulatable supply is denoted by reference numeral 514, and generally comprises an amplifier 516 having a feedback connection to a summer 518, which combines the output of
 30 the amplifier with an input signal. The modulatable DC supply is provided on line 520. An inductor 522 is connected between the output of the transistor power

amplifier 502 and the modulatable power supply on line 520 represents the supply feed inductance.

In accordance with the invention, a control circuit 530 is provided comprising a resonant circuit and a resistive load. The resonant circuit includes an inductor 532 and a capacitor 534, and a load 536 is provided. The control circuit 530 is connected to the output of the transistor power amplifier 502 via an RF blocking circuit 524, comprising an inductor 528 and a capacitor 526 connected in parallel.

The control circuit 530 is connected to ground as represented by 540.

Reference is made herein to high frequencies. The range of values of such high frequencies is application dependent. However in general reference to high frequencies is reference to high modulation frequencies. In a preferred implementation of the invention, in radio frequency applications, the range of high frequencies is at the upper part of the modulation spectrum, but substantially less than the frequency of the radio frequency signal.

Reference is also made herein to low impedance. The range of values of such low impedance is application dependent. In general, the impedance should not be substantially higher at any particular modulation frequency from the average impedance over a range of frequencies. In a preferred implementation, a low impedance is considered to be in the range of 1 to 10 ohms.

Thus, the invention and embodiments thereof provide a control circuit for use at the output of a power amplifier stage which utilises a modulated supply. The control circuit includes a resistor, and preferably a resonant circuit comprising an inductor and a capacitor. The inductor of the resonant circuit may be provided by inherent inductance contained in the output stage of the power amplifier. The provision of such a control circuit overcomes a problem associated with the power amplifier topology.

Embodiments of the invention have been described where the provision of the control circuit is "off-chip", and specifically connected to the metallisation of a printing wiring or circuit board. The invention is not limited to its implementation to such locations. For example, the control circuit may be implemented "on-chip". This gives direct access to the equivalent circuit such as shown in Fig. 2, and therefore may

provide better performance. In Figure 1, reference numerals 118 and 120 denote potential locations of the control circuit on-chip.

The specific values of the elements of the control circuit are implementation dependent. One skilled in the art will be able to choose appropriate values of the capacitor, inductor and resistor of the control circuit in accordance with the application in which it is being used.

In essence, the invention provides for maintaining a low impedance at the drain (output) node of the transistor in the power amplifier circuit such that parasitic resonance in the power amplifier circuit is damped.

The invention has been described herein by way of reference to particular embodiments and examples. The invention is not limited to any of the specific embodiments described. Modifications and variations to the embodiment presented herein will be understood by one skilled in the art. The scope of protection afforded by the invention is defined by the appended claims.

Claims

1. A power amplifier including a resistive element connected at an output thereof to maintain a low impedance at the output across a range of operational frequencies.
2. A power amplifier according to claim 1 further including a transistor for receiving a signal to be amplified at an input and for providing an amplified signal at the output.
3. A power amplifier according to claim 1 or claim 2 wherein the output is adapted for connection to a modulated power supply.
4. A power amplifier circuit according to claim 3 wherein the output is adapted for connection to a modulated power supply via a supply feed inductance.
5. A power amplifier circuit according to any preceding claim wherein said resistive element comprises a resistor.
6. A power amplifier circuit according to any preceding claim further comprising a reactive element connected in series with said resistive element.
7. A power amplifier circuit according to claim 6 wherein said reactive element comprises a capacitive element or an inductive element in series with a capacitive element.
8. A power amplifier circuit according to claim 7 wherein said inductive element comprises a conductive element of said circuit.
9. A power amplifier according to claim 8 wherein said conductive element comprises a part of a conductive track or a bond wire.
10. A power amplifier according to any one of claims 7 to 9 wherein said inductive element comprises an inductor.
11. A power amplifier according to any one of claims 7 to 10 wherein said capacitive element comprises a capacitor.
12. A power amplifier according to any one of claims 2 to 11 wherein the signal to be amplified is a radio frequency signal.
13. A power amplifier circuit comprising a transistor for receiving a signal to be amplified at an input and for outputting an amplified signal at an output; a

modulated power supply connected to the transistor output; and a resistive element connected at the transistor output such that a low impedance is maintained at the transistor output across a range of operational frequencies.

14. A method of maintaining a low impedance across a range of operational frequencies in a power amplifier, the method including providing a resistive element at an output of the power amplifier.

15. A method according to claim 14 further comprising the step of providing a reactive element connected in series with said resistive element.

Abstract

A power amplifier circuit comprising a transistor for receiving a signal to be amplified at an input and for outputting an amplified signal at an output; a modulated power supply connected to the transistor output; and a resistive element connected at the transistor output such that a low impedance is maintained at the transistor output across a range of operational frequencies.

10 [Figure 5]

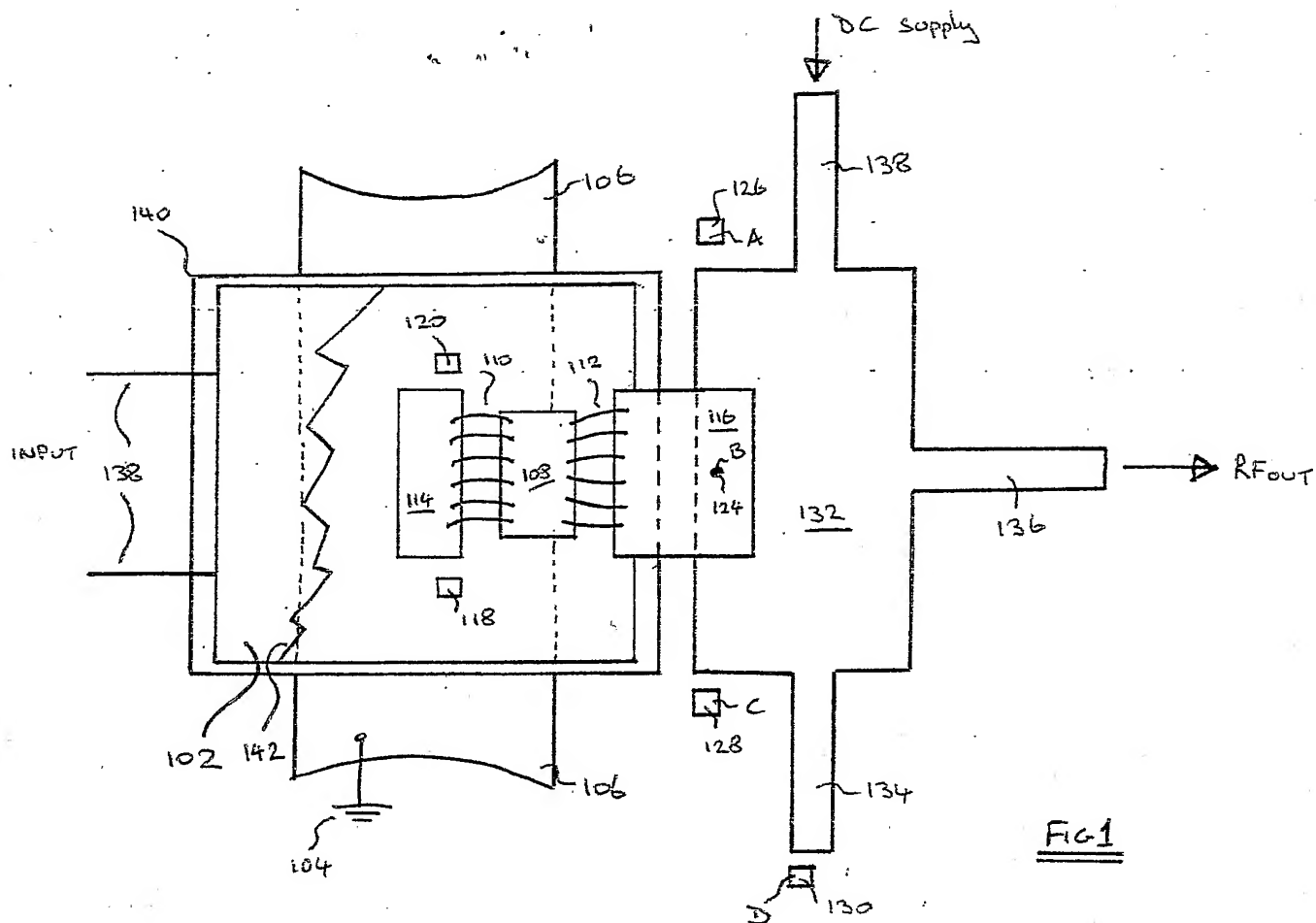


FIG 1

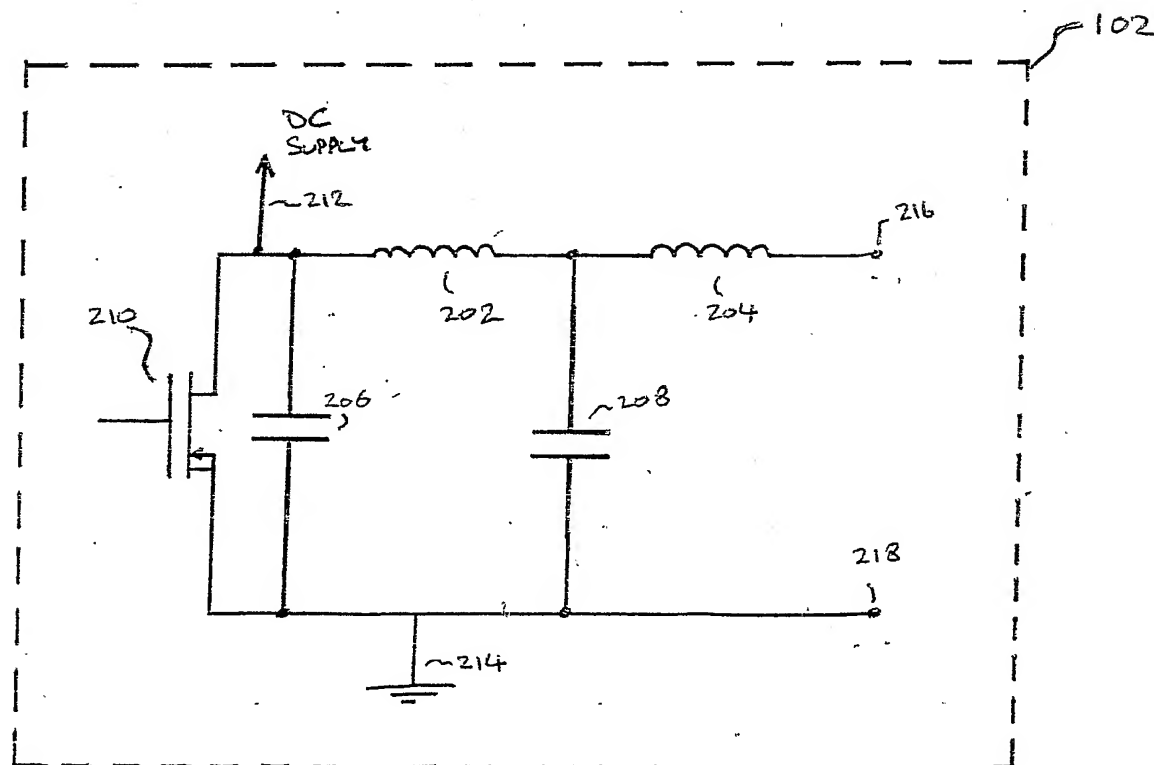


FIG 2

11/11/11



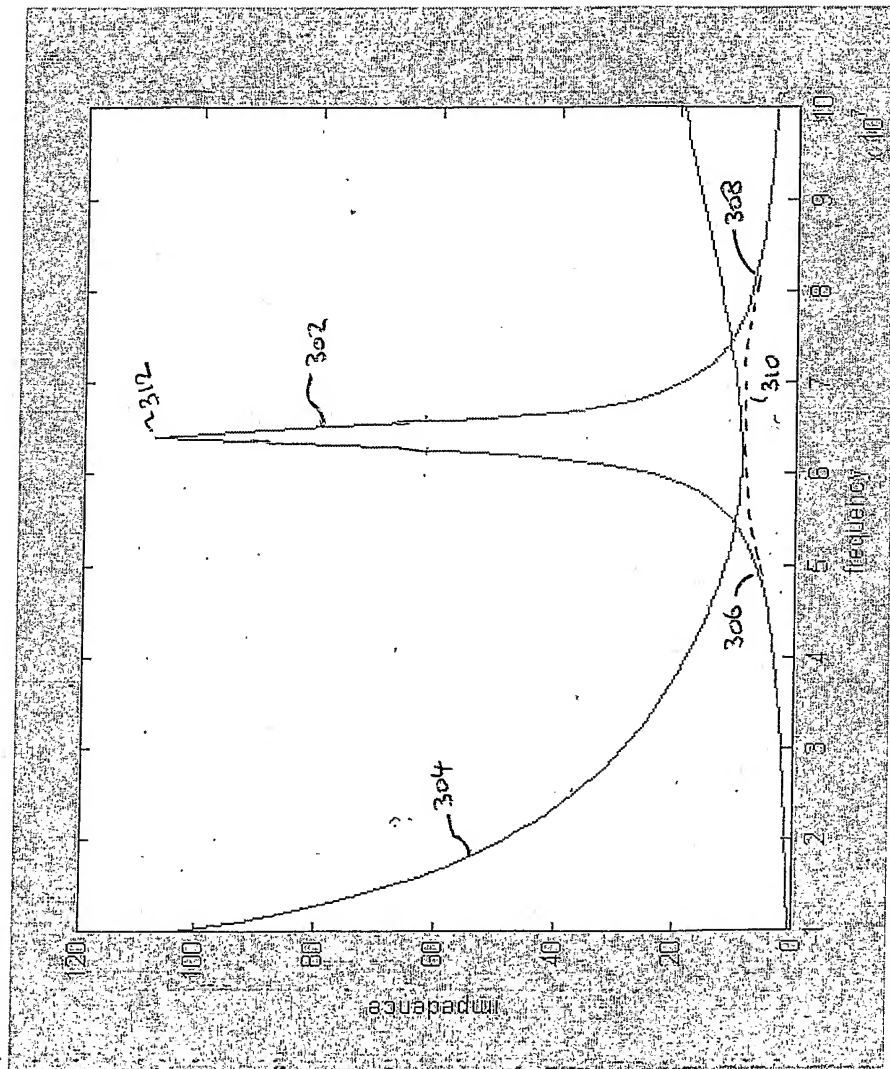
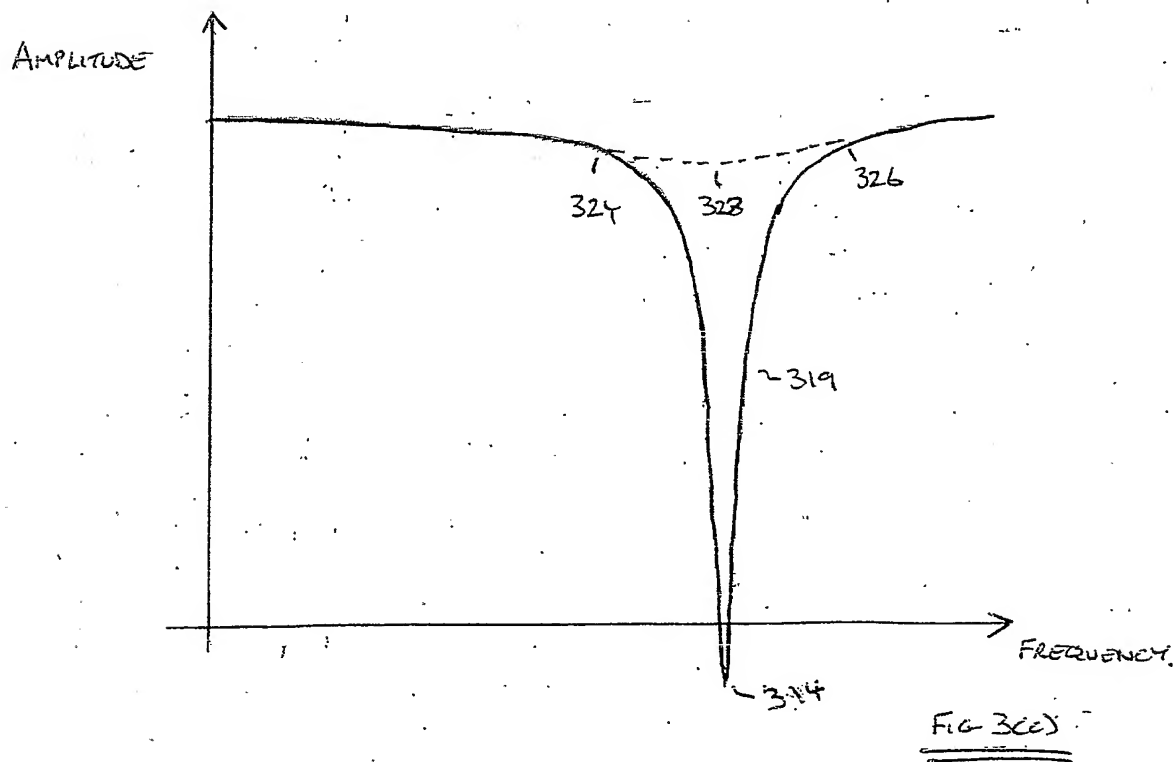
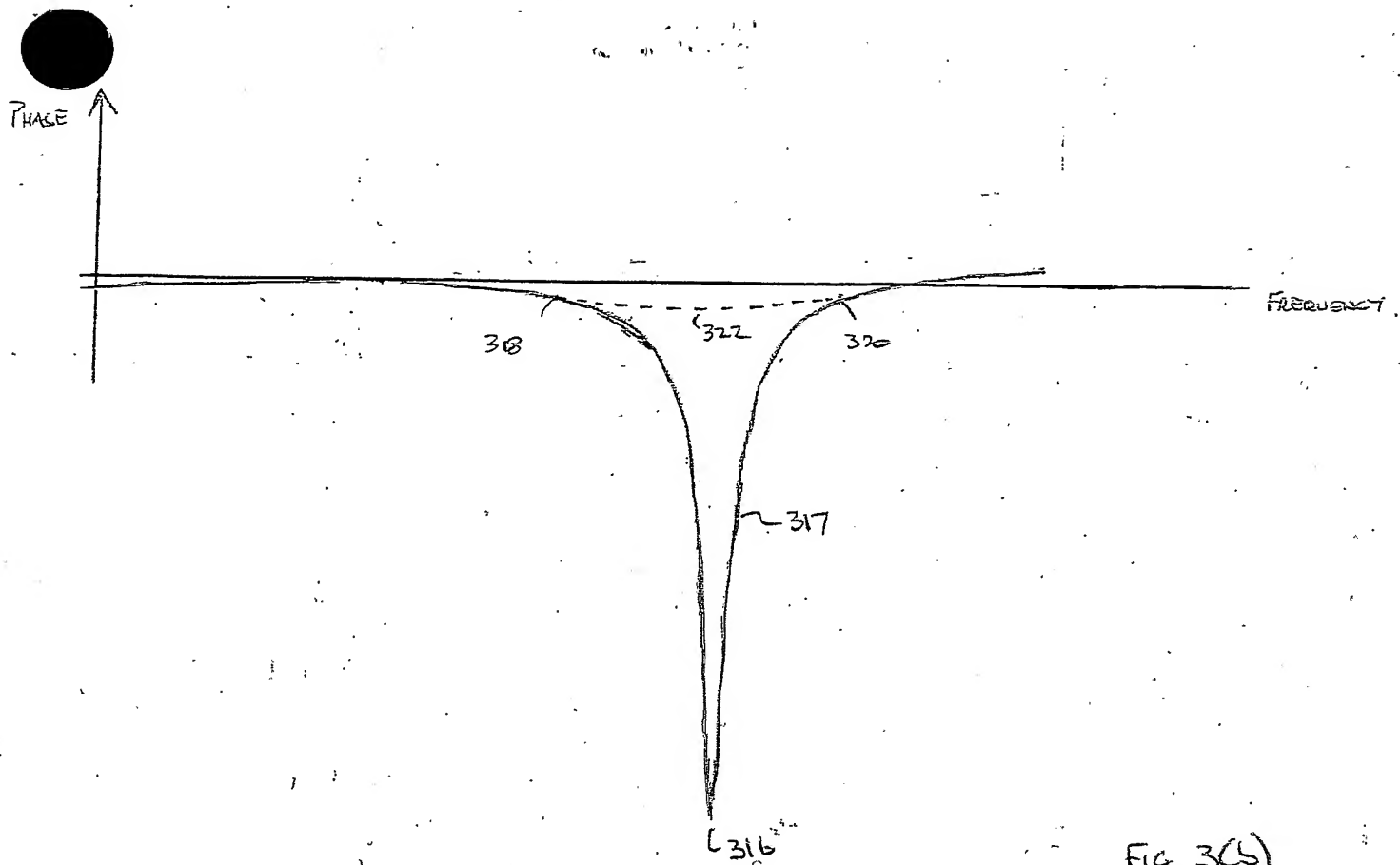


FIG 3(a)

11/11/11







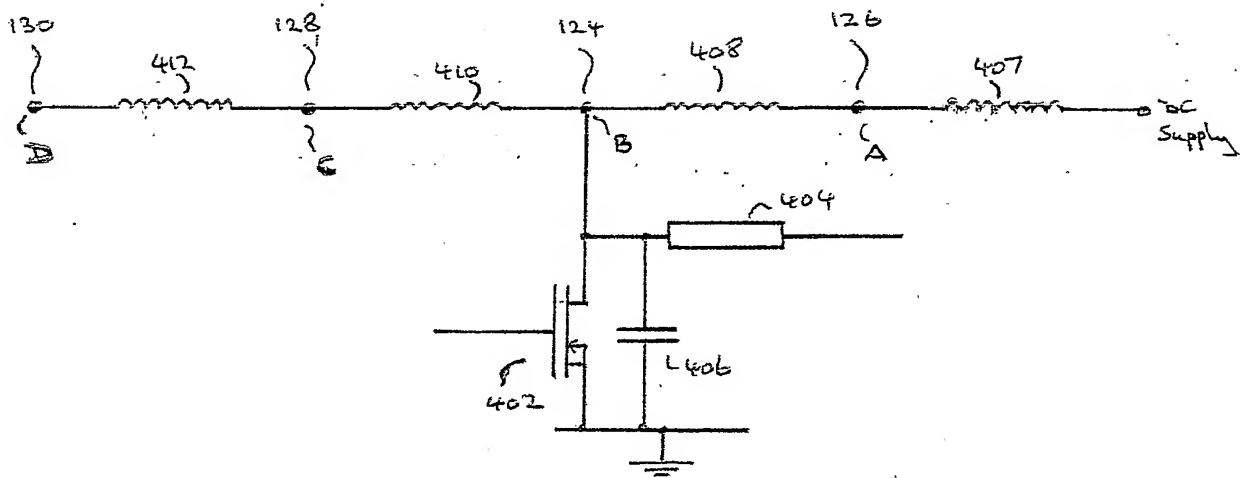


FIG 4(a)

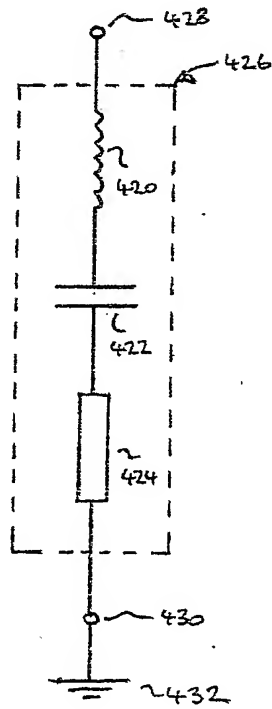
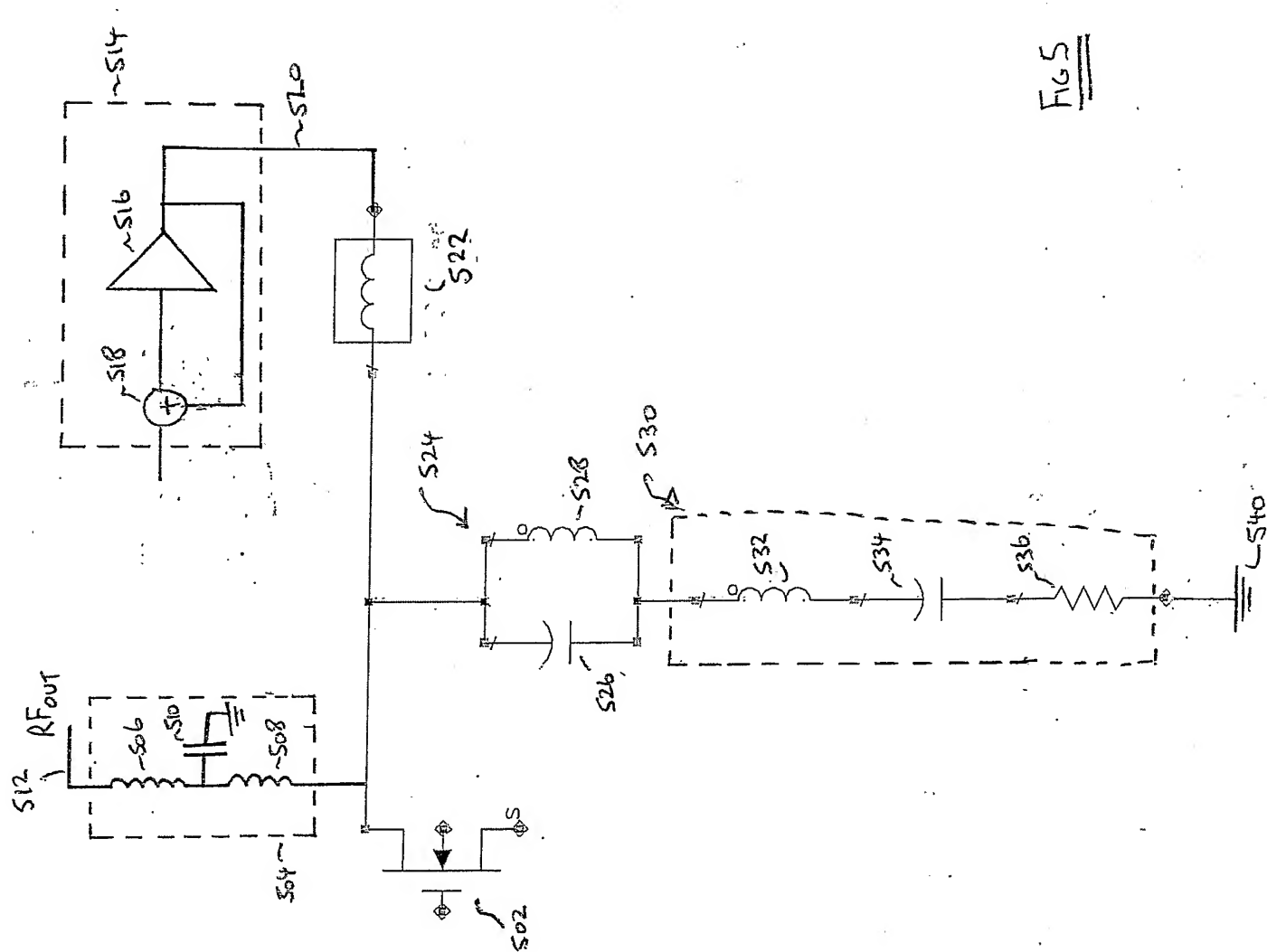


FIG 4(b)





PCT/IB2005/000338

